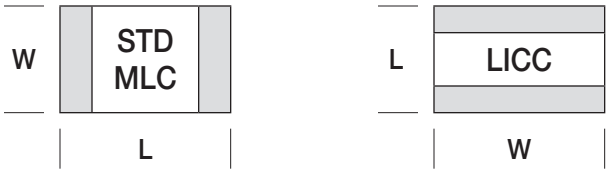
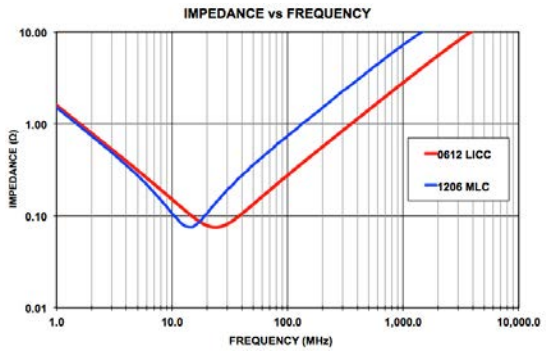
Low Inductance Chip Capacitors (LICC)

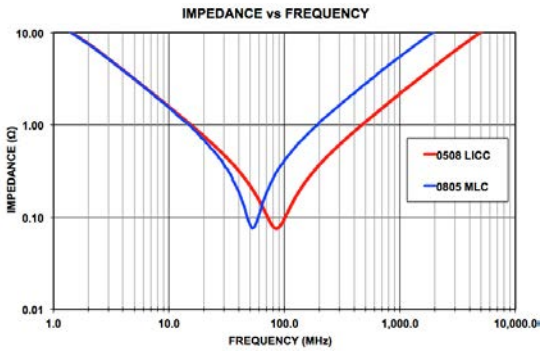
LICC capacitors are specially designed to exhibit lower inductance by altering the aspect ratio of the terminations. The smaller current loop length results in Equivalent Series Inductance (ESL) that is typically 60% lower then standard MLCs of the same size. This ESL improvement is extremely advantageous in the high frequency power decoupling of high speed digital MPU, FPGA, DSP, etc..

Features

- Low Inductance
- High Series Resonant Frequency
- Sn-Pb and Polyterm® Termination Options
- Surface Mount
- Small Size
- RoHS Compliant







Case Size / Available Capacitance

JDI	EIA	MM	DIELECTRIC	10nF	22nF	47nF	0.10uF	0.22uF	0.47uF	1.00uF	2.2uF	4.7uF	10uF
B14	0306	0816	X7R	25V	25V	25V	16V	6.3V					
			X5R				10V	10V	6.3V	6.3V	6.3V		
B15	0508	1220	X7R	50V	50V	25V	25V	16V	6.3V	6.3V			
			X5R						10V	10V	6.3V		
B18	0612	1632	X7R	50V	50V	50V	50V	25V	16V	6.3V			
			X5R							10V	10V	6.3V	6.3V

Please visit our website for complete specifications

How to Order LICC Capacitors

P/N written: 160B14W104MV4T

160	B14	W	104	M	V	4	T
VOLTAGE	SIZE	DIELECTRIC	CAPACITANCE	TOLERANCE	TERMINATION	MARKING	PACKING
6R3 = 6.3 V 100 = 10 V 160 = 16 V 250 = 25 V 500 = 50 V	B14 = 0306 B15 = 0508 B18 = 0612	W = X7R X = X5R	1st two digits are significant; third digit denotes number of zeros 103 = 0.01 µF (10NF) 104 = 0.10 µF	M = ± 20% *Values < 10 pF only	V = NI Barrier with 100% Tin Plating (Matte) T = SnPb	4 = Unmarked (Not available)	E = Embossed 7” T = Punched 7” No code = bulk Tape specs. per EIA RS481